APPENDIX

IN THE CLAIMS

Please amend the claims as follows.

13. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

14. The portable electronic apparatus according to claim 13, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

15. The portable electronic apparatus according to claim 13, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

16. The portable electronic apparatus according to claim 13, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

17. The portable electronic apparatus according to claim 16, wherein said received signal is a modulated signal.

18. (amended) An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said IC card by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

19. The IC card according to claim 18, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

20. The IC card according to claim 18, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

21. The IC card according to claim 18, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

22. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said reader/writer by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

23. The reader/writer according to claim 22, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

24. The reader/writer according to claim 22, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

25. The reader/writer according to claim 22, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

26. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

27. The portable electronic apparatus according to claim 26, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

28. The portable electronic apparatus according to claim 26, wherein said first direction is an increasing direction and said

direction opposite to said first direction is a decreasing direction.

29. The portable electronic apparatus according to claim 26, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

30. An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said IC card by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said

first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

31. The IC card according to claim 30, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

32. The IC card according to claim 30, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

33. An IC card according to claim 30, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

34. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said reader/writer by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

35. The reader/writer according to claim 34, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

36. The reader/writer according to claim 34, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

37. The reader/writer according to claim 34, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.